IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Charles W.C. Lin		
Title:	BUMPLESS FLIP CHIP ASSEMBLY WITH SOLDER VIA		
Serial No.:	Unknown	Filed:	Herewith
Examiner:	Unknown	Group Art Unit:	Unknown
Atty. Docket No.:	P002-2		

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Dear Sir:

Please amend the application as follows.

In the Abstract and Specification

Replace the Abstract and Specification with the enclosed Substitute Specification.

In the Claims

Cancel claims 1-14 without prejudice or disclaimer to the subject matter recited therein.

Add the following claims:

15. A method of making a flip chip assembly, comprising:

attaching a substrate to a semiconductor chip, wherein the substrate includes a dielectric layer and metallization, the dielectric layer includes first and second surfaces that are opposite one another and a via hole that extends between the first and second surfaces, the metallization is disposed on walls of the via hole, the chip includes a terminal pad that is aligned with the via hole, and a reflowable material that contains solder contacts the metallization and the pad; and then

reflowing the reflowable material to provide an electrical connection between the metallization and the pad.

16. The method as recited in claim 15, wherein the reflowable material is deposited on the metallization before attaching the substrate to the chip, and during the reflowing the reflowable material wets and flows on an exposed portion of the pad beneath the via hole.

17. The method as recited in claim 15, wherein the reflowable material is deposited on the pad before attaching the substrate to the chip, and during the reflowing the reflowable material wets and flows on an exposed portion of the metallization in the via hole.

18. The method as recited in claim 15, wherein the pad is directly beneath substantially all surface area defined by the via hole after the attaching.

19. The method as recited in claim 15, wherein the metallization is electrolessly plated on the walls of the via hole.

20. The method as recited in claim 15, wherein the reflowable material fills a bottom portion of the via hole without filling a top portion of the via hole after the reflowing.

21. The method as recited in claim 15, wherein the reflowable material is solder paste.

22. The method as recited in claim 15, wherein the substrate remains at a fixed position relative to the chip during the reflowing.

23. The method as recited in claim 15, wherein substantially all of the reflowable material is within the via hole after the reflowing.

24. The method as recited in claim 15, wherein the metallization and the reflowable material are the only materials in the via hole after the reflowing.

25. A method of making a flip chip assembly, comprising the following steps in the sequence set forth:

providing a substrate that includes a dielectric layer, wherein the dielectric layer includes first and second surfaces that are opposite one another and a via hole that extends between the first and second surfaces;

depositing metallization on walls of the via hole;

depositing solder on the metallization such that the solder is disposed in the via hole;

attaching the substrate to a semiconductor chip that includes a terminal pad, wherein the first surface faces away from the chip, the second surface faces towards the chip, the via hole is aligned with the pad and the solder contacts the pad; and

applying heat to reflow the solder to form a solder joint that contacts and electrically connects the metallization and the pad and prevents the via hole from exposing the pad.

26. The method as recited in claim 25, including depositing the metallization on the walls using electroless plating.

27. The method as recited in claim 25, including depositing the metallization on the walls such that substantially all of the metallization is within the via hole.

28. The method as recited in claim 25, including depositing the metallization on the walls such that the metallization extends along the walls to the first and second surfaces.

29. The method as recited in claim 25, including depositing the metallization on the walls such that the metallization is aligned with the second surface.

30. The method as recited in claim 25, including depositing the solder on the metallization using electroplating.

31. The method as recited in claim 25, including depositing the solder on the metallization using electroless plating.

32. The method as recited in claim 25, including depositing the solder on the metallization using wave soldering.

33. The method as recited in claim 25, including depositing the solder on the metallization using meniscus coating.

34. The method as recited in claim 25, including depositing the solder on the metallization using solder paste printing.

35. The method as recited in claim 25, including depositing the solder on the metallization such that solder extends along the metallization to the first and second surfaces.

36. The method as recited in claim 25, including attaching the substrate to the chip such that the via hole exposes the pad.

37. The method as recited in claim 25, including attaching the substrate to the chip such that the pad is directly beneath substantially all surface area defined by the via hole.

38. The method as recited in claim 25, including attaching the substrate to the chip using an adhesive between the substrate and the chip.

39. The method as recited in claim 25, including attaching the substrate to the chip using a mechanical clamp.

40. The method as recited in claim 25, including applying the heat to reflow the solder using a convection oven.

41. The method as recited in claim 25, including applying the heat to reflow the solder using a laser.

42. The method as recited in claim 25, including applying the heat to reflow the solder using an infrared continuous belt reflow oven.

43. The method as recited in claim 25, including applying the heat to reflow the solder using hot nitrogen gas.

44. The method as recited in claim 25, including applying the heat to reflow the solder using a vapor phase reflow system.

45. The method as recited in claim 25, including applying the heat to reflow the solder such that substantially all of the solder joint is within the via hole.

46. The method as recited in claim 25, including applying the heat to reflow the solder such that the solder joint fills a bottom portion of the via hole without filling a top portion of the via hole.

47 The method as recited in claim 25, including applying the heat to reflow the solder such that the solder wets and covers an exposed portion of the pad.

48. The method as recited in claim 25, including applying the heat to reflow the solder while maintaining the substrate at a fixed position relative to the chip.

49. The method as recited in claim 25, wherein the metallization and the solder joint are the only materials in the via hole after applying the heat.

50. A method of making a flip chip assembly, comprising the following steps in the sequence set forth:

providing a semiconductor chip that includes a terminal pad;

depositing solder on the pad;

attaching a substrate to the chip, wherein the substrate includes a dielectric layer and metallization, the dielectric layer includes first and second surfaces that are opposite one another and a via hole that extends between the first and second surfaces, the metallization is disposed on walls of the via hole and extends along the walls to the first and second surfaces, the via hole is aligned with the pad and exposes the solder, the solder contacts the metallization, the metallization is spaced from the pad, the first surface faces away from the chip, the second surface faces towards the chip, and the substrate is at a fixed position relative to the chip; and

applying heat to reflow the solder such that the solder wets and flows on the metallization in the via hole and forms a solder joint that contacts and electrically connects the metallization and the pad while the substrate remains at the fixed position relative to the chip.

51. The method as recited in claim 50, wherein the metallization is aligned with the second surface.

52. The method as recited in claim 50, wherein essentially all of the solder joint is in the via hole.

53 The method as recited in claim 50, wherein the pad is directly beneath essentially all surface area defined by the via hole after attaching the substrate to the chip.

54. The method as recited in claim 50, wherein the metallization and the solder joint are the only materials in the via hole after applying the heat.

55. A method of making a flip chip assembly, comprising the following steps in the sequence set forth:

providing a substrate that includes a dielectric layer, wherein the dielectric layer includes first and second surfaces that are opposite one another and a via hole that extends between the first and second surfaces;

electrolessly plating metallization on walls of the via hole, wherein the metallization extends along the walls to the first and second surfaces;

electroplating solder on the metallization such that the solder is disposed in the via hole;

attaching the substrate to a semiconductor chip using an adhesive therebetween, wherein the first surface faces away from the chip, the second surface faces towards the chip, the chip includes a terminal pad, the via hole is aligned with and exposes the pad, the solder contacts the pad and the metallization is spaced from the pad; and

applying heat to reflow the solder such that the solder wets and flows on the pad and forms a solder joint that contacts and electrically connects the metallization and the pad and prevents the via hole from exposing the pad.

56. The method as recited in claim 55, wherein the metallization is aligned with the second surface.

57. The method as recited in claim 55, wherein essentially all of the solder joint is in the via hole.

58 The method as recited in claim 55, wherein the pad is directly beneath essentially all surface area defined by the via hole after attaching the substrate to the chip.

59. The method as recited in claim 55, wherein the metallization and the solder joint are the only materials in the via hole after applying the heat.

60. A method of making a flip chip assembly, comprising the following steps in the sequence set forth:

providing a substrate that includes a dielectric layer and a conductive trace, wherein the dielectric layer includes first and second surfaces that are opposite one another and a via hole that extends between the first and second surfaces, and the conductive trace includes metallization disposed on walls of the via hole and a bond site disposed on the first surface and spaced from the via hole;

depositing solder on the metallization and the bond site, wherein the solder on the metallization is in the via hole, the solder on the bond site is outside the via hole, and the solder on the metallization does not contact the solder on the bond site;

attaching the substrate to a semiconductor chip, wherein the first surface faces away from the chip, the second surface faces towards the chip, the chip includes a terminal pad, the solder on the metallization contacts the pad, the metallization does not contact the pad, and the solder on the bond site does not contact the chip; and

applying heat to reflow the solder such that the solder on the metallization forms a solder joint that contacts and electrically connects the metallization and the pad, the solder on the bond site forms a solder contact that does not contact the solder joint and does not contact the chip, and the conductive trace electrically connects the solder joint and the solder contact.

61. The method as recited in claim 60, including depositing the solder on the metallization and the bond site using electroplating.

62. The method as recited in claim 60, including depositing the solder on the metallization and the bond site using electroless plating.

63. The method as recited in claim 60, including depositing the solder on the metallization and the bond site using wave soldering.

64. The method as recited in claim 60, including depositing the solder on the metallization and the bond site using meniscus coating.

65. The method as recited in claim 60, including depositing the solder on the metallization and the bond site using solder paste printing.

66. The method as recited in claim 60, wherein the metallization is aligned with the second surface.

67. The method as recited in claim 60, wherein essentially all of the solder joint is in the via hole.

68. The method as recited in claim 60, wherein the metallization and the solder joint are the only materials in the via hole after applying the heat to reflow the solder.

69. The method as recited in claim 60, wherein the pad is directly beneath essentially all surface area defined by the via hole after attaching the substrate to the chip.

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Abstract and Specification

The Abstract and Specification have been changed as set forth in the enclosed Substitute Specification -Changes Shown.

In the Claims

Claims 1-14 have been canceled, and claims 15-69 have been added.

REMARKS

Claims 15-69 are pending. In this Preliminary Amendment, claims 1-14 have been canceled, and claims 15-69 have been added. In addition, the Abstract and Specification have been amended to improve clarity. No new matter has been added.

In view of the amendments and remarks set forth herein, the application is believed to be in condition for allowance. Should any issues remain, the Examiner is encouraged to telephone the undersigned attorney.

Respectfully submitted,

D Sigmond

David M. Sigmond
Attorney for Applicant
Reg. No. 34,013
(303) 554-8371
(303) 554-8667 (fax)

SUBSTITUTE SPECIFICATION – CHANGES SHOWN

BUMPLESS FLIP CHIP ASSEMBLY WITH SOLDER VIA

CROSS-REFERENCE TO RELATED APPLICATIONS

The present application is continuation of U.S. application number 09/465,024 filed on December 16, 1999, which is an application filed in accordance with 35 U.S.C. §119 and claims the benefit of earlier filed Singapore application number 9804817-6 filed on ~~17~~ December 17, 1998.

1. Field of the Invention

This invention relates generally to a semiconductor device assembly, and in particular, relates to a connection of ~~the~~ integrated circuit (IC) chip or chips to ~~a~~ substrate circuitry, printed circuit board, and interconnect components. ~~More specifically, the present invention relates to a chip assembly that includes a single or multi-layered substrate of which circuitry is connected to the input/output terminal pads of the IC chip through solder reflow in the via apertures or holes. The solder deposition techniques include electrolytic plating, electroless (chemical) plating, wave soldering, meniscus coating and solder printing techniques.~~

2. Background of the Invention

Recent developments of semiconductor packaging suggest an increasingly critical role of the technology. New demands are coming from requirements for more leads per chip and hence smaller input/output terminal pad pitch, shrinking die and package footprints, and higher operational frequencies~~y~~ that generate more heat, thus requiring advanced heat dissipation designs. All of these considerations must be met and, as usual, placed in addition to the cost that packaging adds to the overall semiconductor manufacturing costs.

Conventionally, there are three predominant chip-level connection technologies in use for integrated circuits, namely wire bonding, tape automated bonding (TAB) and flip chip (FC) to electrically or mechanically connect integrated circuits to leadframe or substrate circuitry. Wire bonding has been the far most broadly applied technique in the semiconductor industry because of its maturity and cost effectiveness. However, this process can be performed only one wire bond at a time between the semiconductor chip's bonding pads and the appropriate interconnect points. Furthermore, because of the ever increasing operational frequency of the device, the length of the interconnects needs to be shorter to minimize inductive noise in power and ground, and also to minimize crosstalk

between the signal leads. An example of such a method is disclosed in U.S. Pat. No. 5,397,921 issued to Karnmezos ~~et al~~.

Flip chip technology is characterized by mounting of the unpackaged semiconductor chip with the active side facing down to an interconnect substrate through ~~some kind of~~ contact anchors such as solder, gold or organic conductive adhesive bumps. The major advantage of flip chip technology is the short interconnects which can, therefore, handle high speed or high frequency signals. There are essentially no parasitic elements, such as inductance. Not only is the signal propagation delay slashed, but much of the waveform distortion is also eliminated. Flip ~~c~~Chip also allows an array interconnecting layout that provides more I/O than a perimeter interconnect with the same die size. Furthermore, it requires minimal mounting area and weight which results in overall cost saving since no extra packaging and less circuit board space is used. An example of such a method is disclosed in U.S. Pat. No. 5,261,593 issued to Casson et al.

While flip chip technology has tremendous advantages over wire bonding, its cost and technical limitations are significant. First of all, prior art flip chip technology must confront the challenges of having to form protruded contact anchors or bumps to serve as electrical connections between the integrated circuit chip and substrate circuitry. Examples of such an approach are disclosed in U.S. Pat. No. 5,803,340 issued to Yeh, ~~al.~~ et al. and U.S. Pat. No. 5,736,456 issued to Akram. These approaches typically include a very costly vacuum process to deposit an intermediate under-bump layer that serves as an adhesive and diffusion barrier. This barrier layer is typically composed of a film stack that can be in the structure of chromium/copper/gold. Bumping materials such as solder are subsequently deposited onto this intermediate layer through evaporation, sputtering, electroplating, solder jetting or paste printing methods followed by a reflow step to form the solder contacts. Although evaporation and sputtering ~~techniques~~ can potentially offer high density bumps, these processes need very tight control and normally result in poor yield. As a result, a conventional flip chip assembly is not only very costly but also suffers from very serious reliability problem~~eoncerns~~ and a high fatality ratio.

Techniques for fabricating the intermediate under-bump barrier layer as well as the bump material utilizing electroless plating ~~methods~~ are also known in the prior art. An example of such a method is described in the U.S. Pat. No. 5,583,073 issued to Lin et al. Although the electroless technique provides an economical, simple and effective method

for providing an under-bump barrier layer, contacting material such as solder or adhesive is still required for assembling. Solder dipping or screen printing of solder paste onto these bumps has been explored but has been met with very limited success due to lack of solder bridging control and non-uniform deposition of solder on the metal bumps. This process ~~can be very troublesome and~~ also suffers from poor process control as input/output terminal pad spacinge ~~is~~ gets smallerting ~~closer and closer together~~.

In view of the limitations of currently available integrated circuit assembling methods, a high performance, reliable and economical device and method that can effectively interconnect integrated circuits to the external circuitry would be greatly desirable.

SUMMARY OF THE INVENTION

It is therefore, an object of the present invention to provide a flip chip assembly to address high density, low cost and high performance requirements of semiconductor packaging. The device and method of the present invention involves the bonding of substrate circuitry to a semiconductor device through the reflowing of pre-deposited solder to connect via apertures or holes of the substrate to terminal pads of the semiconductor device without the need for conventional bumps, bonding wire, or other media.

More specifically, the present invention relates to a chip assembly that includes a single or multi-layered substrate of which circuitry is connected to the input/output terminal pads of the IC chip through solder reflow in the via holes. The solder deposition techniques include electrolytic plating, electroless (chemical) plating, wave soldering, meniscus coating and solder printing. ~~To achieve the foregoing, the assembly includes a rigid or flexible dielectric substrate having a plurality of electrically conductive circuitry and a plurality of via apertures or holes. The conductive traces on the surface of the substrate are extended into each specific via hole through the conductive material deposited thereon. This through-hole (PTH) material such as plated copper provides a conductive base for solder deposition or solder wetting. Soldering material such as tin-lead alloy or lead-free solder is pre-deposited in the via hole or on the terminal pad. This readily available solder is to serve as the joint material after the substrate is attached to the semiconductor chip. The orientation of the attachment between chip and substrate circuitry ensures that at least one of the via holes in the dielectric substrate are aligned on~~

the top of the terminal pad.

After alignment, the IC chip is brought in contact with the dielectric substrate through adhesive film or paste, or mechanical techniques. This soft or proximity contact is to ensure that the pre-deposited soldering material is able to reflow into the via hole as well as onto the terminal pad when it is molten. Heat, which serves to activate the flux and bring the solder to its melting point, is used to effect the metallurgical bonding. This re-flow process results in a solder joint which will electrically and physically connect the via hole and IC pad fro permanent contact thereafter. This is important in that it not only assures a very cost effective and simple process, but also provides a compliant joint with significant stress release which results in a very reliable connection between the substrate circuitry and IC chip.

In one embodiment of the invention, the solder pre-deposition is in the via hole. In this embodiment, the via holes are first metallized with a base metal by conventional plated through hole (PTH) technique followed by the various solder deposition techniques. These include electroplating, wave soldering, meniscus solder coating, solder paste printing and dispensing techniques to accomplish the said pre-coating of solder materials onto the metallized hole wall. It is understood from the teaching herein that the particular solder or solder paste and methods of dispensing techniques depicted here is not meant to limit the invention.

In another embodiment of the invention, the solder pre-deposition is on the IC terminal pad. In this method, a barrier layer over-coated on the aluminum pad before solder deposition is preferred. This is to provide a good solder wetting surface and protect the aluminum surface against leaching, oxidation or degradation resulting from heat and soldering contact. This coating can be accomplished by sputtering a stake of thin film or by wet chemical direct plating of electroless nickel and immersion gold. For copper terminal pads, the pre-treatment may not be necessary when its surface is free of oxide and contamination.

The via holes of the substrate circuitry can be formed by various techniques including mechanical drilling, punching, plasma etching or laser drilling. They are formed in the substrate before or after the circuitry patterning depends on the various fabrication processes. The via holes are formed at locations where electrical circuitry on one side of the substrate can be connected to the opposite side of the surface on which the semiconductor chip or chips are mounted and their input/output terminal pads can be

~~aligned thereon.~~

~~A preferred application of heat to reflow pre-deposited solder is by convection oven. Alternatively, the heat may be applied by laser to effect solder reflow and bonding to the IC terminals which are in the vicinity of the via holes. Another example of such an approach is an infrared (IR) continuous belt reflow oven. Alternatively, hot nitrogen gas may be directed onto the solder members of the assembly.~~

In summary, using soldering material directly reflowed between a via hole and a terminal pad can effectively connect an IC chip and dielectric substrate circuitry without external bumps or wires. This approach allows a reliable, low profile, high performance and low cost assembly to be achieved. In particular, a small via hole ~~which can be~~ formed by laser drilling or other techniques allows a very fine pitch terminal pad to be interconnected, which can significantly enhance the capability of packaging future high I/O semiconductor chips.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1A is a fragmented partial sectional side elevational view of a substrate before plating the via hole with solder.

Figure 1B is a fragmented partial sectional side elevational view of the substrate of the type shown in Figure 1A after plating the via hole with solder.

Figure 1C is a fragmented partial sectional side elevational view of a semiconductor chip~~die~~ having a terminal pad.

Figure 1D is a fragmented partial sectional side elevational view of a chip assembly after a semiconductor chip~~die~~ of the type shown in Figure 1C has been attached to a substrate of the type shown in Figure 1B.

Figure 1E is a fragmented partial sectional side elevational view of the chip assembly of the type shown in Figure 1D after a solder reflow process.

DETAILED DESCRIPTION OF THE INVENTION

The bumpless flip chip assembly of the present invention includes a rigid or flexible dielectric substrate having a plurality of electrically conductive circuitry traces and a plurality of via apertures or holes. The conductive traces on the surface of the substrate ~~are~~ extended into the~~each specific~~ via holes through the conductive material deposited on the via hole walls~~thereon~~. This plated through-hole (PTH) material such as plated copper, gold, nickel, titanium or palladium provides a conductive base for solder deposition or

solder wetting. Soldering material such as tin-lead alloy or lead-free solder is pre-deposited in the via hole or on the terminal pad. This readily available solder serves as the joint material after the substrate is attached to the semiconductor chip. The orientation of the attachment between the chip and substrate circuitry ensures that at least one of the via holes in the dielectric substrate isare aligned with a terminal pad.

After alignment, the IC chip is brought in contact with the dielectric substrate through an adhesive film or paste, or mechanical techniques such as mechanical clamping. This soft or proximity contact is to ensures that the pre-deposited soldering material is able to reflow into the via hole as well as onto the terminal pad when it is molten. Heat, which serves to activate the flux and bring the solder to its melting point, is used to effect the metallurgical bonding. This re-flow process will results in a solder joint which will electrically and physically connects the via hole and IC pad for permanent contact thereafter. This is important in that it not only assures a very cost effective and simple process, but also provides a compliant joint with significant stress release which results in a very reliable connection between the substrate circuitry and IC chip.

As defined herein, the preferred embodiment is particularly directed to the bonding of an integrated circuit (IC) chip to a flexible circuitized substrate, or to a more rigid, circuitized substrate, a particular example of the latter being a printed circuit board. It is to be understood, however, that the invention is not limited to the attachment to printed circuit boards, in that other circuitized substrates, including known plastic and ceramic substrates, may be employed. Typically, an organic-type substrate is preferable for the purpose of lower cost, and superior dielectric property whereas an inorganic-type of substrate is preferable when high thermal dissipation and matched coefficient of expansion are desired. TBy the term "substrate" as used herein is defined as at least one layer of dielectric material having at least one conductive layer thereon. Printed circuit boards of similar type are well known in the electronics industry, as well as the processes for making the same, and therefore, further definition is not believed to be necessary. Such structures may include many more electrically conductive layers than those depicted in FIGS. 1A through 1E, depending on the desired operational characteristics. As is known, such electrically conductive layers may function as signal, power, and/or ground layers.

In one embodiment of the invention, the solder pre-deposition is in the via hole. In this embodiment, the via holes are first metallized with a base metal by a conventional

plated through hole (PTH) technique followed by ~~the various~~ solder deposition ~~techniques~~. Solder deposition techniques~~These~~ include electroplating, electroless plating, wave soldering, meniscus solder coating, solder paste printing and dispensing ~~techniques~~ to accomplish the ~~said~~ pre-coating of solder materials onto the metallized hole wall. It is understood ~~from the teaching herein~~ that the particular solder or solder paste and methods of dispensing ~~techniques~~ depicted herein are ~~is~~ not meant to limit the invention.

In another embodiment of the invention, the solder pre-deposition is on the IC terminal pad. In this method, a barrier layer over-coated on an~~the~~ aluminum pad before solder deposition is preferred. This is to provide a good solder wetting surface and protect the aluminum surface against leaching, oxidation or degradation resulting from heat and soldering ~~-~~contact. This coating can be accomplished by sputtering a stake of thin film or by wet chemical direct plating of electroless nickel and immersion gold. For copper terminal pads, the pre-treatment may not be necessary when the~~its~~ surface is free of oxide and contamination.

The via holes of the substrate ~~circuitry~~ can be formed by various techniques including mechanical drilling, punching, plasma etching or laser drilling. They are formed in the substrate before or after the circuitry patterning dependings on the various fabrication processes. The via holes are formed at locations ~~where electrical circuitry on one side of the substrate can be connected to the opposite side of the surface on which the semiconductor chip or chips are mounted and their input/output terminal pads can be aligned thereon~~ that can be aligned with and expose input/output terminal pads of the semiconductor chip or chips that are subsequently mounted on the side of the substrate opposite the side where the electrical circuitry is formed.

A preferred application of heat to reflow pre-deposited solder is by a convection oven. Alternatively, the heat may be applied by a laser to effect solder reflow and bonding to the IC terminal pads which are in the vicinity of the via holes. Another example of such an approach is an infrared (IR) continuous belt reflow oven. Alternatively, hot nitrogen gas may be directed onto the solder members of the assembly. It is understood ~~from the teaching herein~~ that the particular re-flow techniques depicted above ~~is~~ are not meant to limit the invention, in that it is also possible to reflow the solder using a~~by~~ vapor phase reflow system.

If the finished product is, for instance, a ball grid array package, solder balls will

normally be placed on the specific trace~~pads~~ on the surface of the dielectric substrate. This finished package can be connected to a printed circuit board by reflowing the solder balls to form an attachment to the conductor~~traces~~ of the printed circuit board.

FIGS. 1A to 1E are diagrammatic cross-sectional views showing steps involved in the manufacturing of an integrated circuit assembly by pre-depositing solder in the substrate via hole and re-flowing the solder to connect the terminal pad.

Referring initially to FIG. 1A, a substrate 101 having a plurality of electrically conductive circuitry traces 102 partially covered by the solder mask 103 is shown. The traces 102 on the substrate 101 extend into a plurality of via holes 104 by a thin layer of plated through-hole copper 105 deposited on the via hole walls~~thereon~~.

FIG. 1B shows the substrate 101~~is~~ immersed in a solder plating solution and a layer of solder 106 is electroplated on the metallized via hole wall as well as on the solder opening site.

FIG. 1C shows an integrated circuit chip 107 having various types of transistors, wires and the like (not shown), which has a plurality of exposed input/output terminal pads 108. These pads 108 are formed~~were deposited~~ with a stake of thin film 109 in the structure of titanium (500 Angstroms)/nickel (700 Angstroms)/gold (1000 Angstroms) to serve as the barrier and adhesive layer. Passivation is disposed on chip 107 outside pads 108.

FIG. 1D shows IC chip 107 securely attached to the substrate ~~circuitry~~ 101 by adhesive paste ABLESTIK "ABLEBOND 961-2" 110 to form an assembly 111. The orientation of the attachment is arranged in such a manner that a~~the~~ specific terminal pad 108 of the integrated circuit chip 107 is in contact with the solder 106 inside a specific via hole 104. The via hole 104 ~~is to~~ serves as an~~the~~ electrically connecting channel~~s~~ for the respective trace~~s~~ 102 of the substrate 101.

FIG. 1E shows the input/output terminal pad 108 firmly joined together with a specific via hole 104 by solder joint 112 to become an integral part after the assembly 111 i~~was~~ placed in an oven that causes~~for a~~ solder 106 to reflow. This simultaneously-reflowed joint 112 provides an effective ~~means for~~ electrical and mechanical connection~~s~~ between IC chip 107 and substrate~~the dielectric circuitry~~ 101. The soldering material 113 deposited in the solder mask opening serves as the contacting material for the next level assembly.

Though only one integrated circuit chip 107 is shown ~~in the figure~~, it is to be understood that additional integrated circuit chips, as well as passive components such as resistors or capacitors, can also be mounted on the substrate ~~circuitry~~ 101.

Likewise ~~Though only one solder system is shown in the figure~~, it is to be understood that many solder systems including lead-free ones; can also be applied and serve the connection purpose.

The present invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. The presently disclosed embodiments are, therefore, to be considered in all respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims and all changes which come within the meaning and range of equivalency of the claims are, therefore, to be embraced therein.

What is claimed is:

BUMPLESS FLIP CHIP ASSEMBLY WITH SOLDER VIA

ABSTRACT

A flip chip assembly, and methods of forming the same, including a single or multi-layer substrate having a plurality of via ~~apertures or~~ holes which serve as the connection between the semiconductor device and substrate circuitry. The method of manufacturing the flip chip assembly includes~~device of the present invention may include~~ the steps of attaching an integrated circuit (IC) chip having a plurality of input/output terminal pads~~or chips~~ to a rigid or flexible substrate ~~circuitry~~ having a plurality of via~~through~~ holes. These via~~through~~ holes are aligned with the ~~IC~~ terminal pads so that the respective traces on the substrate can be connected to the respective ~~input/output~~ terminal pads through the via holes. After attachment, the pre-deposited solder inside the via holes or on the terminal pads is re-flowed. This re-flow soldering process ~~will then~~ electrically connects the IC chip to the substrate ~~circuitry to the semiconductor device and therefore complete the connection~~. The solder~~ing materials~~ can be deposited by plating, wave soldering, meniscus coating, and screen printing techniques.

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Examiner:	Unknown	Group Art Unit:	Unknown
Atty. Docket No.:	P002-2		

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

SUBMISSION OF PROPOSED DRAWING AMENDMENT FOR APPROVAL BY EXAMINER

Attached please find a copy of the original Figures 1A and 1B with red ink markings showing the proposed changes to the drawings in the above-identified application in accordance with 37 C.F.R. § 1.123. The Examiner's approval for these changes is requested.

Respectfully submitted,

David M. Sigmond
Attorney for Applicant
Reg. No. 34,013
(303) 554-8371
(303) 554-8667 (fax)

FIG. 1A

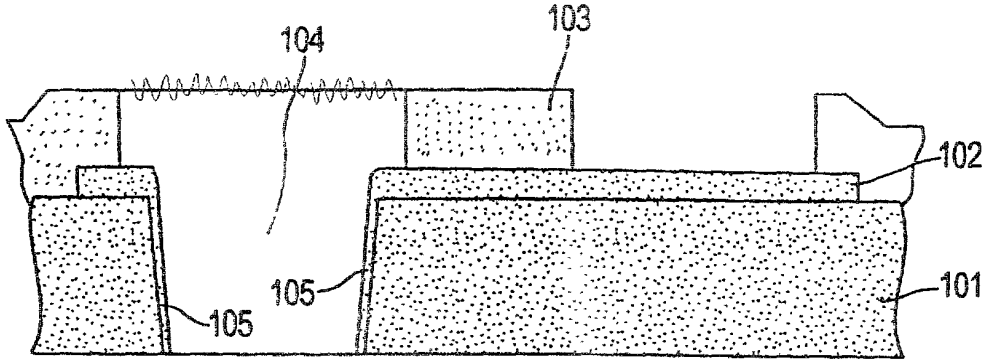

FIG. 1B